Applicants:	Walter Fix et al.
Serial No.:	10/562,869
Filed:	April 7, 2006
For:	Logic Gate with a Potential-Free Gate Electrode for Organic Integrated Circuits
Examiner:	Eva Y. Montalvo Art Unit: 2814
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APPEAL BRIEF

MS Appeal Brief
Commissioner for Patents
Box 1450
Alexandria, VA 22313-1450

This is an appeal from the final rejection dated July 16, 2010 rejecting claims 1, 3 and 8, all of the active claims in the application, claims 2, and 4-7 being canceled. The Commissioner is authorized to charge deposit account 03 0678 for the $540.00 appeal brief fee and any other fee that might be due for this paper or credit any over payments.

REAL PARTIES IN INTEREST

PolyIC GmbH & Co. KG of Furth, Germany is the assignee of the above-entitled application.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences with respect to the above-entitled application.

STATUS OF CLAIMS

Claims 1, 3 and 8 are pending, stand finally rejected, and are before the Board of Appeal. Claims 2 and 4-7 are canceled. The rejected claims are listed in the Appendix attached hereto.

STATUS OF AMENDMENTS

An amendment submitted in response to the Final Rejection was not entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In one advantageous embodiment of the organic logic gate of the present invention, the gate electrode of the charging FET (field effect transistor) is capacitively coupled to a source electrode of the charging FET. Page 2, lines 29-31.

In another advantageous refinement of the organic logic gate, the drain electrode of the charging FET is capacitively coupled to a gate electrode of the charging FET. Page 2, lines 31-34.

It is thus possible, with a relatively low outlay, for the gate electrode to be coupled to one of the other terminals of the charging FET in order to improve the switching behavior of the logic gate. Page 2, lines 34-37.

The capacitive coupling between the gate electrode and one of the other terminals of the FET makes it possible, given a suitable design of the charging FET and the coupling capacitance, to improve the switching properties of the logic gate. The present invention makes it possible for organic logic gates to function or to switch rapidly and stably even at low supply voltages (below 10 v). page 2, line 37 to page 3, line 7.

In the case of a capacitive coupling between the gate electrode and source or drain electrode of a charging FET, it is possible to dispense with a direct electrical coupling between the two electrodes. Page 3, lines 25-28.

Another refinement of an organic logic gate is constructed without plated-through holes. Page 3, lines 24-25.

The organic logic gate is characterized in that the capacitive coupling is achieved by means of the gate electrode of the charging FET being capacitively coupled to the source electrode of the charging FET. Page 8, lines 13-16 (claim 2 of the original claims).

The organic logic gate is characterized in that the capacitive coupling is achieved by means of the gate electrode overlapping the source electrode of the charging FET. Page 8, lines 19-22 (claim 3 of the original claims). The organic logic gate is characterized in that the capacitive coupling is achieved by means of the drain electrode overlapping the gate electrode of the charging FET, page 8, line 37 to page 9, line 2.

The capacitance 16 may be implemented by the gate electrode overlapping the source or drain electrode. Page 6, lines 14-16.

Fig. 4, illustrates a cross section through a charging transistor FET in accordance with the present invention. The charging FET is applied on a carrier material or on a substrate 22, which may comprise glass, plastic, crystal or a similar material. Page 6, lines 28-32.

Two electrodes 8 and 12 of the charging FET are applied on the substrate 22. One of the electrodes 8, 12 is the source electrode and one electrode is the drain electrode. Page 6, lines 35-37.

The two electrodes 8, 12 are connected by a semiconductor layer 24. An insulator layer 26 is arranged above the semiconductor layer 24. The gate electrode 20 is arranged above the insulator layer 24. In this case, the region 4 essentially defines the charging transistor and the region 16 essentially defines the region of the capacitive coupling between the gate electrode 20 and the electrode 8. Page 7, lines 5-11.

Fig. 4 discloses solely a capacitor formed by a portion of the gate 20 overlying the electrode 8. The capacitor is coupled to the gate electrode and one of the source/drain electrodes 8, 12 of an FET transistor as shown in the figure. One of ordinary skill in the electronics art would understand the disclosed capacitor in Fig. 4 as applying a potential at the disclosed gate and the potential is solely provided by the capacitor shown in the figure. No other elements are shown in this figure notwithstanding other elements could be included, which the specification describes as being shown in Figs. 2 and 3 and described elsewhere in the specification as different embodiments of the disclosed invention as expressly stated in the specification. These other embodiments include a resistor in parallel with that capacitor.

See page 4, lines 16-28, describing an alternative embodiment "In another preferred embodiment of the invention, the gate electrode of the charging FET . . . " This embodiment is described in connection with figures 2 and 3, not claimed.

Claim 1 of the original filed claims (see the Appendix) calls for:

> An organic logic gate comprising at least one charging field effect transistor (charging FET) having source, drain and gate electrodes and at

least one switching field effect transistor (switching FET), the charging FET having at least one gate electrode, a source electrode and a drain electrode, characterized in that the gate electrode of the charging FET is not connected via an electrical line to a voltage source. (underlining added)

Support for the appealed claim 1 subject matter calling for:

"wherein the gate electrode of the charging FET is directly capacitively coupled to one of the source/drain electrodes of the charging FET to thereby provide a potential at the gate electrode of the charging FET solely via the capacitive coupling" (underlining added)

is expressly provided by the above sections of the specification, especially Fig. 4, as would be understood by one of ordinary skill in this art to whom the application is directed, and, further, in view of the rest of the filed specification and drawings describing the other embodiments, and the originally filed claims, especially the underlined portion, when viewed in their entirety.

THE GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. The objection to the specification as failing to provide antecedent basis for the claimed subject matter as underlined above.

2. The rejection of claims 1,3 and 8 under 35 USC 112, 1st paragraph as failing to comply with the written description requirement in that the claimed subject matter is not described in the specification in such a way as to reasonably convey to one of ordinary skill that the inventors at the time the application was filed had possession of the claimed invention in that the underlined portion of claim 1 is not disclosed in the drawings or written description.

The Action states that claims 1, 3 and 8 would be allowable if the rejection under 35 USC 112, 1st paragraph is overcome.

ARGUMENT

The two grounds of the rejection are basically directed to the same issue, which is that there is no support for the claim 1 subject matter as follows and, in particular, the underlined portion, and thus this is new matter:

> "wherein the gate electrode of the charging FET is directly capacitively coupled to one of the source/drain electrodes of the charging FET to thereby provide a potential at the gate electrode of the charging FET solely via the capacitive coupling" (underlining added)

Applicants submit this subject matter is not new matter, is permitted under the law and by the MPEP as discussed below as would be understood by one of ordinary skill. Patent applications and their claims are directed to those of ordinary skill in the electronics art who would have no problem in construing the present claim 1 as finding full support in the specification and would understand what is involved according to the filed specification.

One possible reason for the rejection is that the claim term as underlined does not expressly appear identically verbatim anywhere in the specification, i.e. the ground of rejection:

> "The objection to the specification as failing to provide antecedent basis for the claimed subject matter as underlined above."

and similarly as the basis of Ground 2 of the rejection. However, such verbatim use of claim terms is not important as discussed below in connection with a relevant Federal Circuit decision on this point.

The objected to term only appears in the amended claim. However, this lack of corresponding terminology in the specification is of no concern and is not determinative as to whether or not there is support for the added claim term in the specification. Identity of terminology in the claims and specification is not the law as held by that Federal Circuit case.

Fig. 4 plainly shows an FET transistor solely with a capacitor coupled between one of the source electrodes and gate electrode as claimed in claim 1. One of ordinary skill in the electronics art would understand that the disclosed capacitor of Fig. 4 will in fact, as a normal functioning device as known in the art, will and can provide a potential at the gate as claimed. The original filed claim 1 in fact expressly states that the gate electrode of the charging FET is not connected via an electrical line to a voltage source. The specification consistent with this, states "In the case of a capacitive coupling between the gate electrode and source or drain electrode of a charging FET, it is possible to dispense with a direct electrical coupling between the two electrodes." Page 3, lines 25-28.

A capacitive coupling is well known as not forming a direct electrical coupling. This corresponds to original claim 1 in that the gate electrode of the charging FET is not connected via an electrical line to a voltage source. The fact that the capacitive coupling as not forming a direct electrical coupling to the gate electrode terminology is not expressly stated as being implemented solely by a capacitor in the specification and drawings is of no moment. One of ordinary skill knows that the specification and original claim 1 terminology is referring to a solely connected capacitor as claimed in claim 1.

What is at issue is what the specification and drawings teach one of ordinary skill in the electronics art. Such a person is well versed in circuit design, the nature and function of various electronic components such as resistors, inductors, capacitors, diodes, transistors and numerous other electronic components as used in the electronics art. These components are manufactured to specifications provided by manufacturers and are widely distributed to those of skill in the art and to the public at large. There is no mystery in what constitutes a capacitance, and how it operates in a given circuit and as to the fact it does not provide a direct electrical coupling between electrical terminals.

Fig. 4 shows such a capacitor and only a capacitor. One of ordinary skill is taught by Fig. 4, claim 1, and the corresponding specification text, by way of example, that the disclosed FET has, in one embodiment, solely a capacitor connected to the device gate electrode and to one of the FETs source/drain electrodes. This structure is plainly alluded to by the so called one embodiment disclosed in the specification at page 2, lines 29-31 (Summary of the Claimed Subject Matter).

The specification also teaches solely a capacitor in the sections identified above (Summary of the Claimed Subject Matter) as follows:

The drain electrode of the charging FET is capacitively coupled to a gate electrode of the charging FET. Page 2, lines 31-34. The capacitive coupling between the gate electrode and one of the other terminals of the FET makes it possible, given a suitable design of the charging FET and the coupling capacitance, to improve the switching properties of the logic gate. The present invention makes it possible for organic logic gates to function or to switch rapidly and stably even at low supply

voltages (below 10 v). page 2, line 37 to page 3, line 7. These sections teach to one of ordinary skill that it is the capacitive coupling that improves the switching properties of the logic gate. This means that the capacitive coupling alone is sufficient to do this as would be understood by one ordinary skill. A resistance is not mentioned here and since it serves some other function, it would be plainly optional as would be understood by such a skilled person.

In the case of a capacitive coupling between the gate electrode and source or drain electrode of a charging FET, the specification states that it is possible to dispense with a direct electrical coupling between the two electrodes, consistent with the original filed claim 1, which refers to the one embodiment with only a capacitive coupling and means that a resistor as shown in Figs. 2 and 3, is optional. Page 3, lines 25-28. This section is especially apropos in that one of ordinary skill would understand that the term "direct electrical coupling" refers to an ohmic coupling, i.e., a resistive or otherwise an electrical conductor that directly conductively connects one element to another element so that a current on the one element is instantly conducted to the other element at all times. A capacitor works differently, is not optional as is the resistor, as is plain from the specification and, most importantly, is an important component resulting in the desired faster switching times. The resistance is only of minor significance to this aspect based on the specification.

The term "to dispense with a direct electrical coupling" means that in the embodiment with solely a capacitive coupling, the so called direct coupling may be eliminated, i.e., a resistive coupling. That is, there is only capacitive coupling intended by this section of the specification. If there is only capacitive coupling and not resistive

coupling, then by definition there is solely only a capacitance involved in the circuit, which suggests that the resistances of Figs. 2 and 3, being optional, may be dispensed with. When the specification states that the resistances may be dispensed with, it is referring to Figs. 2 and 3, as would be understood by those of ordinary skill,

At page 4, lines 16-28, the specification also describes another embodiment. The term "another embodiment" clearly means to one of ordinary skill that there is also a further embodiment in addition to the embodiment at issue involving solely a capacitor coupled between the FET gate and source or drain electrode. This other embodiment is the disclosure of an FET with a capacitor and the optional resistor coupled in parallel between the gate electrode and one of the source electrodes as described in the specification and as shown in Figs. 2 and 3.

Thus, there are two generic embodiments described, the first being that described at page 3, lines 10-33, the claim 1 embodiment manifesting solely a capacitor coupled to the gate with a direct coupling dispensed with (without the optional resistance). The other embodiment in the alternative is the resistive-capacitance parallel coupling between the gate electrode and one or the other of the source/drain electrodes, page 4, lines 16-28. The first embodiment is also shown in Fig. 4, a cross sectional view of a transistor showing solely a capacitor connected to one of the source/drain electrodes. However, there is no circuit diagram of this first embodiment. But that diagram is not necessary as one of ordinary skill would understand its nature (eliminate the resistances of Figs. 2 and 3). The other embodiment is shown by Figs. 2 and 3, which are circuit diagrams.

The fact that only the embodiment with the resistor and capacitor in parallel is shown in a circuit diagram, figures 2 and 3, does not mean that the other embodiment not shown with a corresponding circuit diagram is missing in the specification entirely. This is not true. The embodiment of Fig. 4 is misconstrued by the Examiner as not depicting the embodiment with only the capacitor connected to the involved electrodes. Figure 4 is a depiction of the claim 1 structure that is asserted as missing in that the application does not disclose what is claimed. This is error.

One of ordinary skill is capable of discerning the embodiment of solely a capacitor as claimed by merely visualizing Figs. 2 and 3 without the resistor. This is not a complex circuit wherein such would not be plainly understood. This is a simple circuit. Such a person is not without common sense.

The specification refers to figure 4 as incorporating the embodiments of Figs 2 and 3. This may have been confusing to the Examiner in that the text does not refer expressly to the claimed embodiment in respect of this figure. This claimed embodiment would be understood to be present and thus inherently, if not expressly disclosed. One of ordinary skill in the art would understand the Figs. 2 and 3 as comprising further embodiments involving the optional resistance, and Fig. 4 comprises the first embodiment depicted at the specification page 3 with a further suggestion of modification to that of Figs. 2 and 3. Since only two embodiments are described and only one is shown in Figs. 2 and 3 as a circuit diagram, it would be obvious and common sense to one of ordinary skill to eliminate the obviously optional resistance in these figures. The Examiner misplaces this description as not describing the first embodiment without the parallel resistance in place in error.

The Examiner may have confused these Fig. 2 and 3 drawing descriptions in connection with Fig. 4 as being the only embodiment represented by Fig. 4. This is not what is intended. Merely because a circuit diagram of only the capacitor involved between the gate and one of the source/drain electrodes as claimed is not shown, but only a cross section of the device, does not mean that the claimed invention is not disclosed. The Fig. 4 cross section of the FET device is an express disclosure of the claimed embodiment of claim 1. One of ordinary skill would not be so confused and would understand these disclosures for what they represent as two distinct embodiments. That is all that 35 USC 112 requires.

As to the point that the claim terms are not identically in the specification is of no moment. See *In re Wright*, 9 USPQ32d 1649 (Fed. Cir. 1989). In this case, a similar if not identical issue to that in the instant appeal is discussed. Because 35 USC 112 does not require that the specification describe the invention in words identical to the patent claims, the Court held that the PTO erred in rejecting the patent application whose specification did not include the words "not permanently fixed" added later to the patent claims.

The Examiner rejected all of the claims, explaining that the new limitation added to the claims constituted 'new matter' which was not supported by a sufficient disclosure in the specification required by 35 USC 112 similar to the instant issue. The Examiner questioned whether the applicant unequivocally teaches the absence of permanently fixed microcapsules and this was sustained by the Board of Appeals.

The Court reversed holding that the claimed subject matter need not be described in haec vervba in the specification to satisfy the description requirement of 35

USC 112. The fact that the words "not permanently fixed" are not in the specification is not important according to the Court. The Court said these are common garden variety words known to every English speaking person. The Court reviewed the specification and concluded that the term was described in the original disclosure and that the specification unequivocally teaches the absence of permanently fixed microcapsules. In a similar manner the instant application unequivocally teaches a charging FET whose gate electrode is directly capacitively coupled to one of the source/drain electrodes of the charging FET to thereby provide a potential at the gate electrode of the charging FET solely via the capacitive coupling.

In addition, the terminology in issue is inherent, notwithstanding applicants believe it is expressly disclosed, in the application. As to inherency, reference is made to the MPEP 2163.07(a), which states:

> By disclosing in a patent application a device that inherently performs a function or has a property, operates according to a theory or has an advantage, a patent application necessarily discloses that function, theory or advantage, even though it says nothing explicit concerning it. The application may later be amended to recite the function, theory or advantage without introducing prohibited new matter. *In re Reynolds*, 170 USPQ 94 (CCPA 1971). *In re Smythe*, 178 USPQ 279 (CCPA 1973).

As discussed above, the specification expressly states in the Summary of the Claimed Subject Matter:

> In one advantageous embodiment of the organic logic gate of the present invention, the gate electrode of the charging FET (field effect transistor) is capacitively coupled to a source electrode of the charging FET. Page 2, lines 29-31.
>
> In another advantageous refinement of the organic logic gate, the drain electrode of the charging FET is capacitively coupled to a gate electrode of the charging FET. Page 2, lines 31-34.

> In the case of a capacitive coupling between the gate electrode and source or drain electrode of a charging FET, it is possible to dispense with a direct electrical coupling between the two electrodes. Page 3, lines 25-28. (underlining added in all of the above)

The embodiment wherein the direct electrical coupling is dispensed with includes a circuit such as that of Figs. 2 and 3 wherein the resistor is suggested as being eliminated by the latter of the above-identified clauses and by Fig. 4. The elimination of that resistor manifests the dispensing with the proscribed direct electrical coupling that is plainly disclosed as being one possible arrangement. Fig. 4 reinforces this embodiment as a cross section of solely the capacitor and FET device that would be coupled in a circuit such as Figs. 2 and 3, but wherein a resistor is eliminated. This description necessarily inherently, if not expressly, describes the added claim language as one embodiment. Therefore, the addition of this terminology to the claims is not new matter. The Examiner should be reversed.

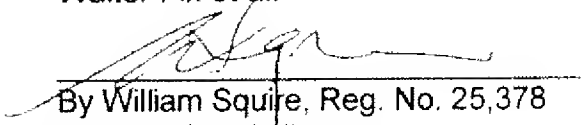
The amendment after final rejection, not in issue in this appeal, attempted to add the circuit diagrams of Figs. 2 and 3 without the resistor therein and also add an amended specification describing such circuit diagrams. Also the title was changed as requested by that Final Action. By reversing the Examiner, this amendment would then be proper for entry and the application then should be in condition for allowance.

CONCLUSION

Applicants have shown that the specification and drawings include an embodiment that supports the objected to claim terminology. The terminology is supported in the specification as shown and the technology represented by such

terminology is inherently, if not expressly, disclosed in the application. The Examiner should be reversed, and all claims allowed. The amendment after final rejection should then be revisited by the Examiner, entered and the application allowed.

Respectfully submitted,
Walter Fix et al.



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APPENDIX-CLAIMS ON APPEAL

1. An organic logic gate comprising:

a circuit having an input and an output and comprising at least one organic charging field effect transistor (charging FET) on a substrate;

the charging FET including a first structured layer comprising source and drain electrodes;

followed by a semiconductor layer on the electrodes followed by a layer of insulating material on the semiconductor layer and adjacent to and contiguous with a second electrode layer forming a gate electrode; and

at least one switching organic field effect transistor (switching FET) having at least one gate electrode, a source electrode and a drain electrode;

the drain-source electrodes of the charging and switching transistors being arranged to be coupled in series between a voltage source and a reference potential such that the gate electrode of the charging FET is not connected via an electrical line directly to a voltage source, to the reference potential, to the input or to the output;

wherein the gate electrode of the charging FET is directly capacitively coupled to one of the source/drain electrodes of the charging FET to thereby provide a potential at the gate electrode of the charging FET solely via the capacitive coupling.

3. The organic logic gate as claimed in Claim 1 wherein the capacitive coupling is achieved by the gate electrode of the charging FET overlapping one of the source/drain electrodes of the charging FET.

8. The organic logic gate as claimed in Claim 1 wherein the organic logic gate is constructed without plated-through holes.

EVIDENCE APPENDIX
CLAIMS AS ORIGINALLY FILED

1. An organic logic gate comprising at least one charging field effect transistor (charging FET) having source, drain and gate electrodes and at least one switching field effect transistor (switching FET), the charging FET having at least one gate electrode, a source electrode and a drain electrode, characterized in that the gate electrode of the charging FET is not connected via an electrical line to a voltage source.

2. The organic logic gate as claimed in claim 1, characterized in that the gate electrode of the charging FET is capacitively coupled to the source electrode of the charging FET.

3. The organic logic gate as claimed in Claim 2, characterized in that the capacitive coupling is achieved by means of the gate electrode overlapping the source electrode of the charging FET.

4. The organic logic gate as claimed in one of the preceding claims characterized in that the gate electrode of the charging FET is resistively coupled to the source electrode of the charging FET.

5. The organic logic gate as claimed in one of the preceding claims characterized in that the gate electrode of the charging FET is capacitively coupled to the drain electrode of the charging FET.

6. The organic logic gate as claimed in claim 5, characterized in that the capacitive coupling is achieved by means of the drain electrode overlapping the gate electrode of the charging FET.

7. The organic logic gate as claimed in Claim 1, characterized in that the gate electrode of the charging FET is resistively coupled to the drain electrode of the charging FET.

8. The organic logic gate as claimed in Claim 1, characterized in that the organic logic gate is constructed without plated-through holes.

RELATED PROCEDINGS EVIDENCE

None